

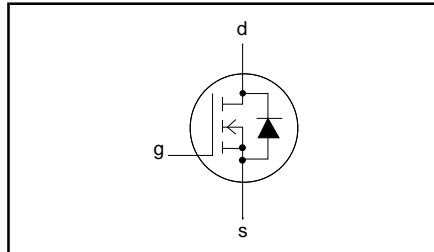
N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 200 \text{ V}$
$I_D = 7.6 \text{ A}$
$R_{DS(ON)} \leq 230 \text{ m}\Omega$

GENERAL DESCRIPTION

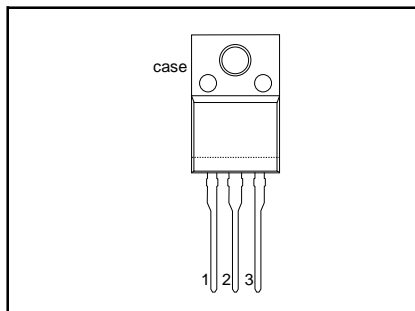
N-channel enhancement mode field-effect power transistor in a plastic full pack envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHX14NQ20T is supplied in the SOT186A (FPAK) conventional leaded package.

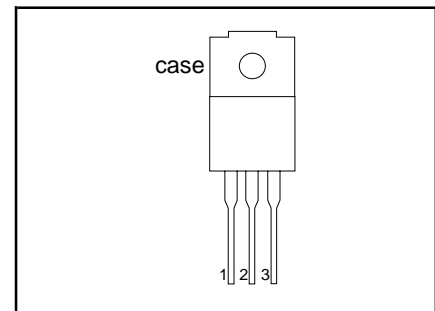
PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A (FPAK)



SOT186 (FPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $150 \text{ }^\circ\text{C}$	-	200	V
V_{DGR}	Drain-gate voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $150 \text{ }^\circ\text{C}$; $R_{GS} = 20 \text{ k}\Omega$	-	200	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	$T_{hs} = 25 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	7.6	A
		$T_{hs} = 100 \text{ }^\circ\text{C}$; $V_{GS} = 10 \text{ V}$	-	4.8	A
I_{DM}	Pulsed drain current	$T_{hs} = 25 \text{ }^\circ\text{C}$	-	30	A
P_D	Total power dissipation	$T_{hs} = 25 \text{ }^\circ\text{C}$	-	30	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	$^\circ\text{C}$

N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 14$ A; $t_p = 38$ μ s; T_j prior to avalanche = 25°C; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig 15	-	70	mJ
I_{AS}	Peak non-repetitive avalanche current		-	14	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-hs}$	Thermal resistance junction to mounting base	SOT186A package, in free air	-	-	4.17	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	55	-	K/W

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$	200 178	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 150^\circ\text{C}$ $T_j = -55^\circ\text{C}$	2 1 -	3 - -	4 - 6	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 7$ A $V_{GS} = 10$ V; $I_D = 7$ A; $T_j = 150^\circ\text{C}$	- -	150 -	230 540	m Ω m Ω
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 7$ A	6	12.1	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 10$ V; $V_{DS} = 0$ V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200$ V; $V_{GS} = 0$ V $T_j = 150^\circ\text{C}$	-	0.05 -	10 500	μ A μ A
$Q_{g(tot)}$	Total gate charge	$I_D = 14$ A; $V_{DD} = 160$ V; $V_{GS} = 10$ V	-	38	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	13.3	-	nC
t_{don}	Turn-on delay time	$V_{DD} = 100$ V; $R_D = 10$ Ω ; $V_{GS} = 10$ V; $R_G = 5.6$ Ω Resistive load	-	25	-	ns
t_r	Turn-on rise time		-	40	-	ns
t_{doff}	Turn-off delay time		-	83	-	ns
t_f	Turn-off fall time		-	31	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die Measured from source lead to source bond pad	-	4.5	-	nH
L_s	Internal source inductance		-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	1500	-	pF
C_{oss}	Output capacitance		-	128	-	pF
C_{rss}	Feedback capacitance		-	60	-	pF

N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

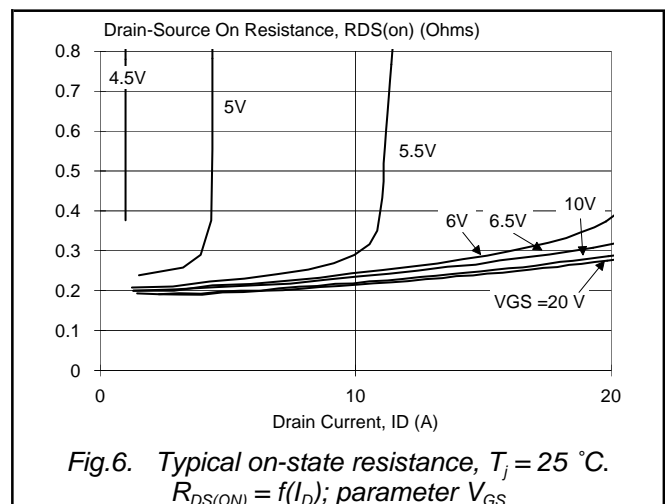
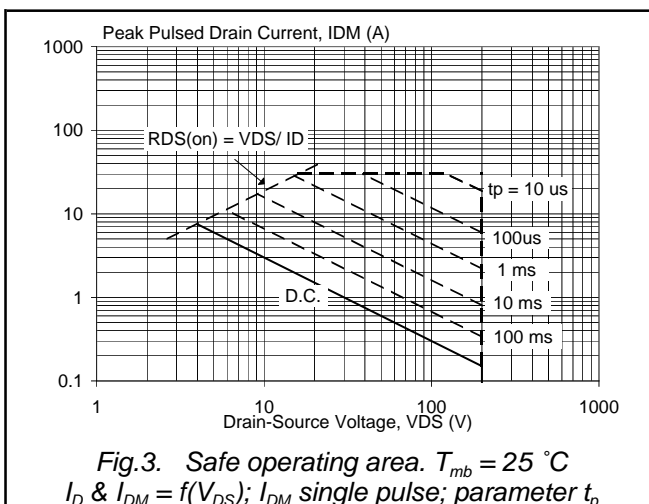
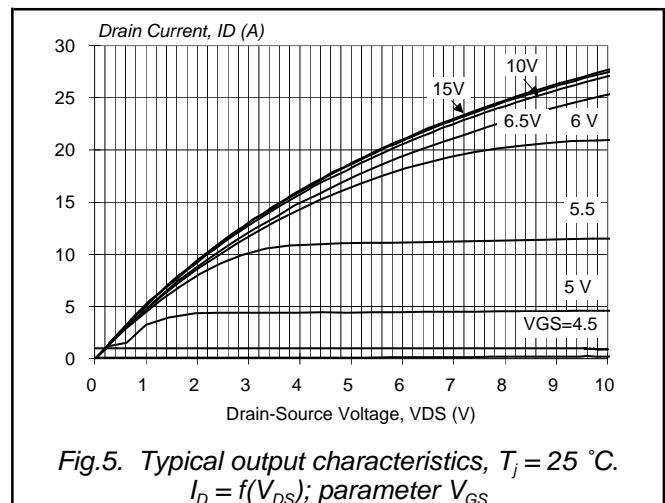
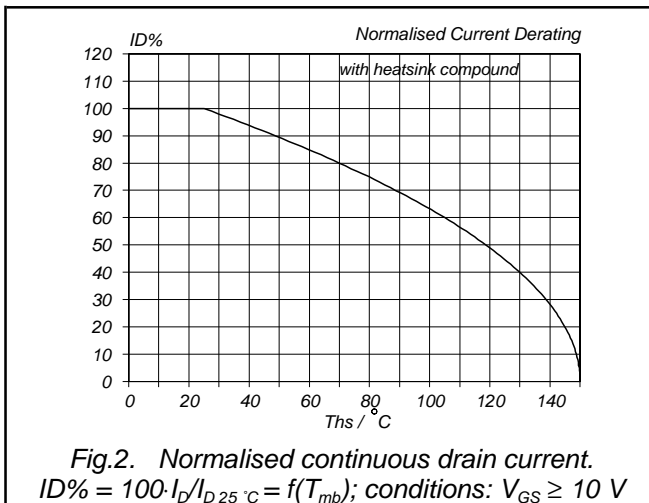
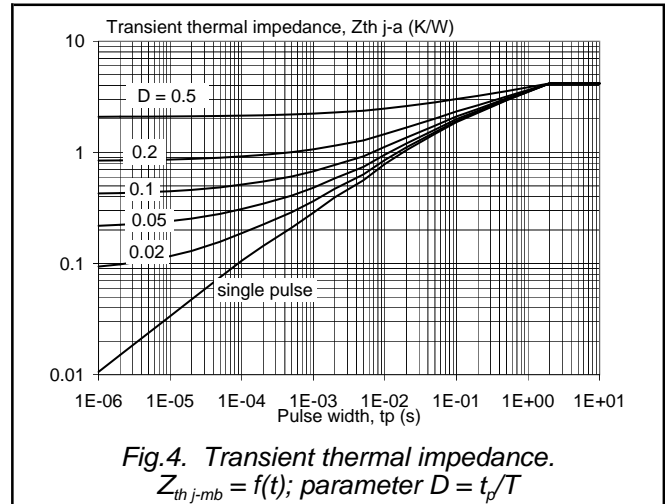
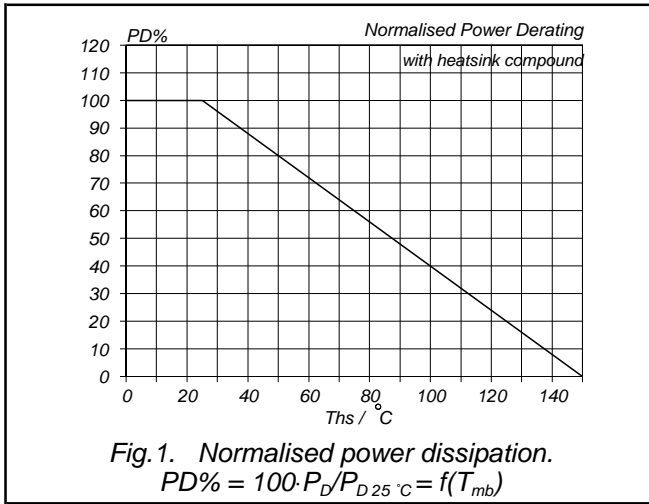
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	14	A
I_{SM}	Pulsed source current (body diode)		-	-	56	A
V_{SD}	Diode forward voltage	$I_F = 14\text{ A}; V_{GS} = 0\text{ V}$	-	1.0	1.5	V
t_{rr}	Reverse recovery time	$I_F = 14\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$	-	135	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	690	-	nC

ISOLATION LIMITING VALUE & CHARACTERISTIC $T_{hs} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	SOT186A package; $f = 50\text{-}60\text{ Hz}$; sinusoidal waveform; R.H. $\leq 65\%$; clean and dustfree	-		2500	V
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	SOT186 package; R.H. $\leq 65\%$; clean and dustfree	-		1500	V
C_{isol}	Capacitance from pin 2 to external heatsink	$f = 1\text{ MHz}$	-	10	-	pF

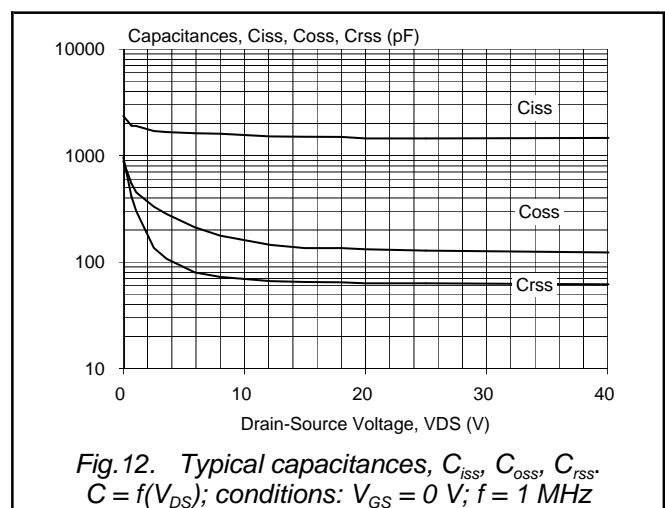
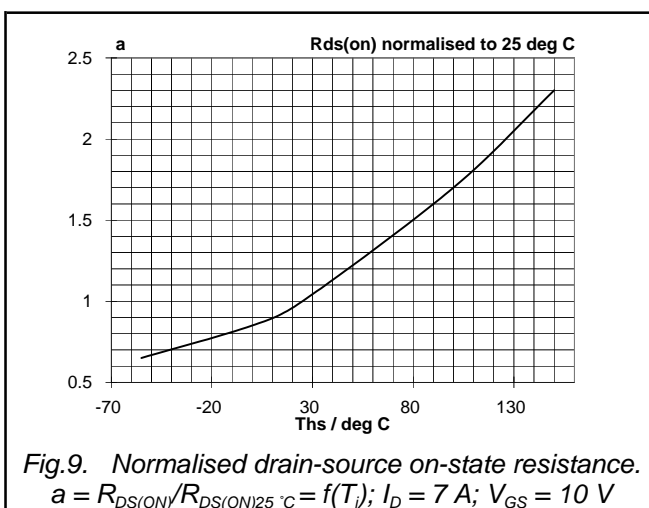
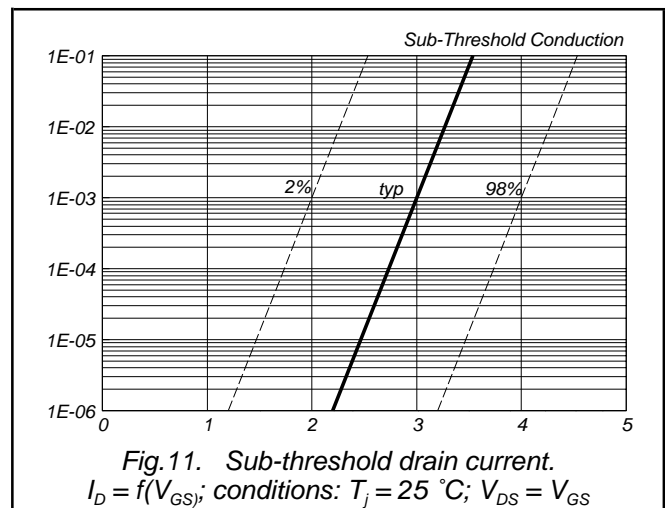
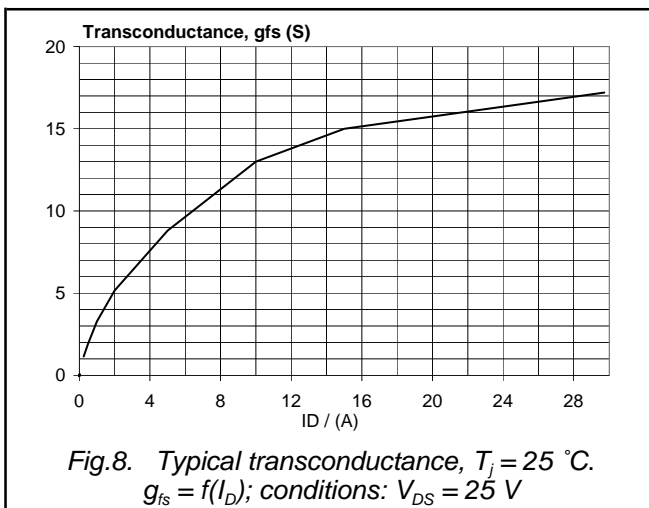
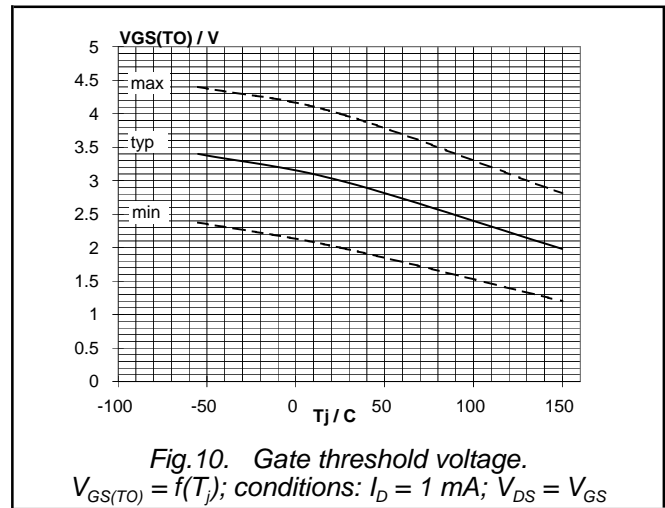
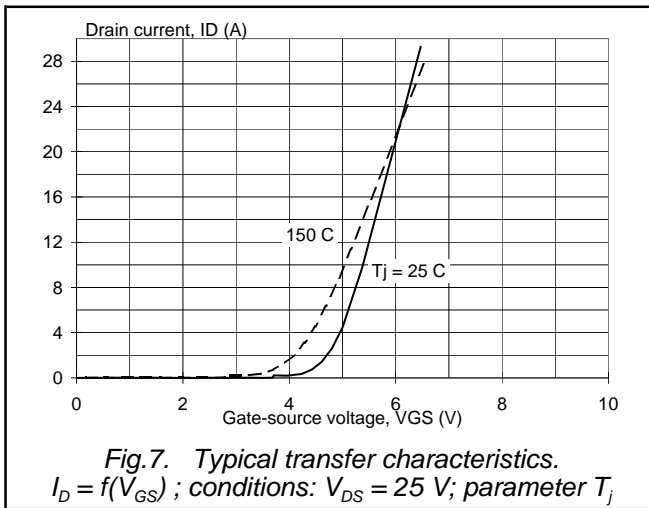
N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T



N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T



N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T

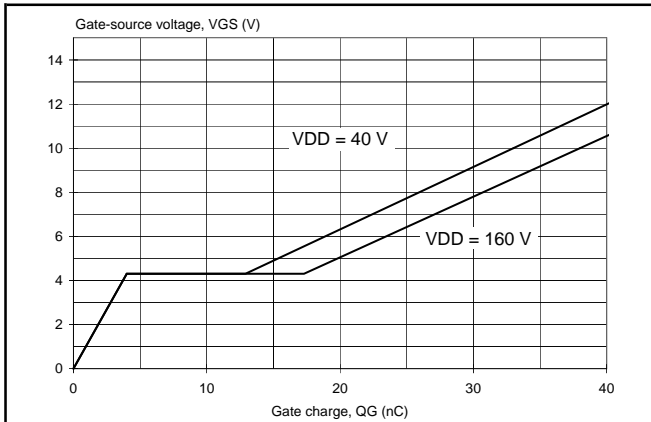


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 14$ A; parameter V_{DS}

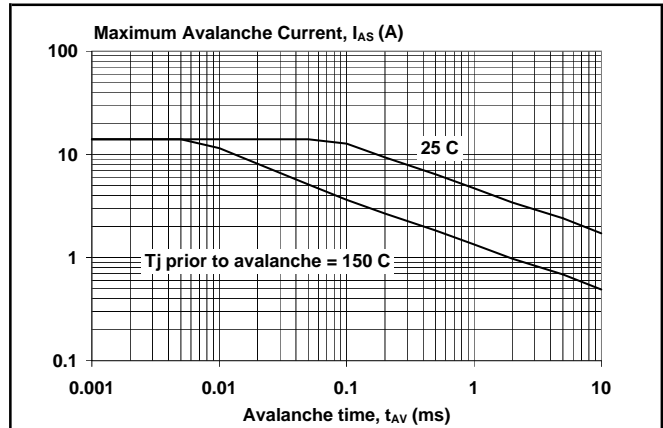


Fig. 15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_{AV}); unclamped inductive load

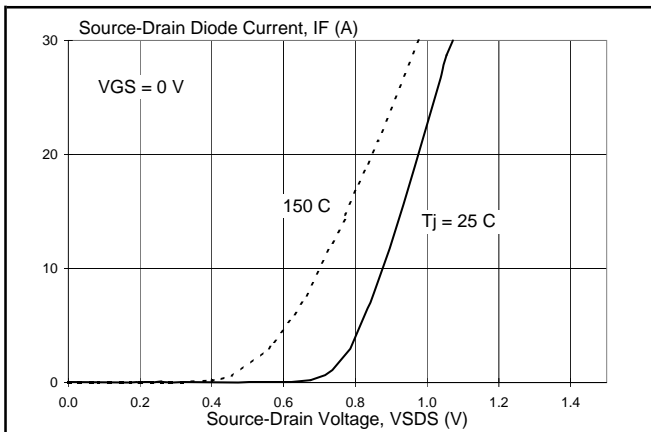


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T

MECHANICAL DATA

Dimensions in mm Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 SOT186A

Net Mass: 2 g

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	T ⁽²⁾	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.2	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 2.3	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

- Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
- Both recesses are $\varnothing 2.5 \times 0.8$ max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186A		TO-220				97-06-11

Fig. 16. SOT186A; The seating plane is electrically isolated from all terminals.

Notes

- Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
- Refer to mounting instructions for F-pack envelopes.
- Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T

MECHANICAL DATA

Dimensions in mm

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 exposed tabs

SOT186

Net Mass: 2 g

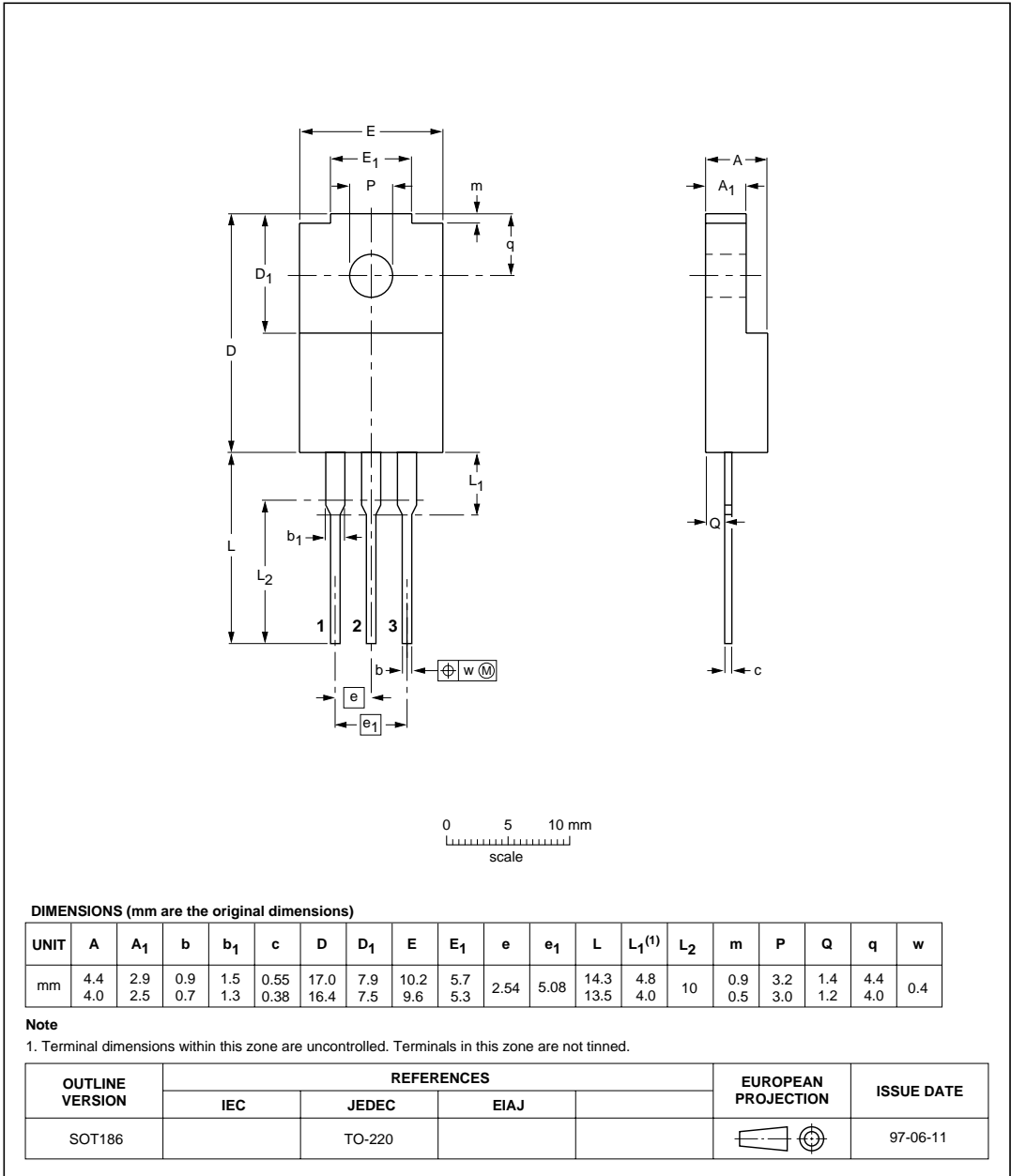


Fig. 17. SOT186; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOS™ transistor

PHX14NQ20T , PHF14NQ20T

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 2000	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.